RoHS Compliant

Industrial Micro SD 3.0

Specifications

November 3rd, 2011

Version 1.0

FEATURES:

- **Fully compatible with SD Card Association specifications**

  - Part 1, Physical Layer Specification, Version 3.1 Final

  - Part 3, Security Specification, Version 3.0 Final

- **Capacity range**

  - 4, 8, 16 GB

- **Performance***

  - Sustained Read: Up to 20 MB/sec

  - Sustained Write: Up to 14 MB/sec

- **SD-protocol compatible**

- **Supports SD SPI mode**

- **Backward compatible with 2.0**

- **Upgradable to Micro SDHC via FAT32**

- **NAND Flash Type: MLC**

- **Operating frequency: up to 100 MHz**

- **Intelligent endurance design**

  - Built-in advanced ECC algorithm

  - Implements global wear-leveling algorithms to substantially increase longevity of flash media

  - Flash bad-block management

  - Built in write protect

  - Copyright protection mechanism: SDMI standard compatible

- **Temperature ranges**

  - Operating temperature: -25 ~ +85°C

  - Storage temperature: -40°C ~ +85°C

- **Operating voltage: 2.7V ~ 3.6V**

- **Physical dimension :** 15mm(L) x 11mm(W) x 1mm(H)

- **RoHS Compliant**

*Vary from capacities. Performance values presented here are typical and may vary depending on settings and platforms.

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1. General Description

As the demand of reliable and high-performance data storage in a small form factor increases, Apacer's Micro SD card 3.0 is designed specifically for multiple applications by offering high endurance, reliability, and agility, where extreme traceability, enhanced data integrity, and exceptionally velocity are required.

The Micro SD 3.0 card fully complies with SD Card Association standard. The Command List is compatible with [Part 1 Physical Layer Specification Ver3.1 Final] definitions, while the Card Capacity of Non-secure Area, Secure Area supports [Part 3 Security Specification Ver3.0 Final] Specifications Regarding its operation efficiency, it can operate at maximum frequency up to 100 MHz and is able to alternate communication protocols between SD and SPI modes. For data read/write speed, the card can perform up to 19 MB/sec.

The card also comes with endurance features for data error detection and correction, ESD protection, built-in permanent/temporary write protection, password protection, and SDMI standard compliant copyright protection mechanism.

1.1 Product Function Block

The Micro SD contains a card controller and a memory core for the SD standard interface.
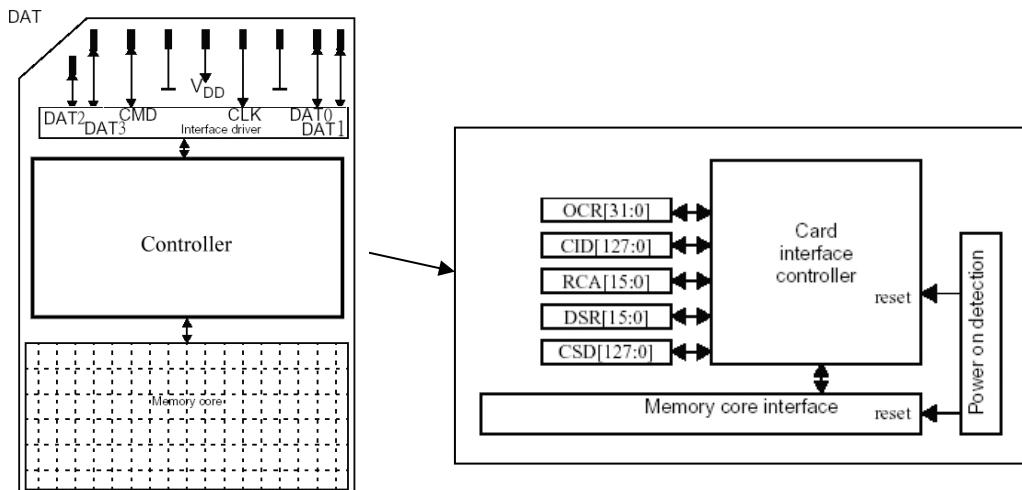
1.2 Functional description

The Micro SD device contains a high level, intelligent flash management that provides many capabilities including:

- Host independence from details of erasing and programming flash memories.

- Powerful ECC algorithms

- Global wear-leveling algorithms

- Power management for low power operation

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1.2.1 Flash Management

The SD controller contains logic/physical flash block mapping and bad block management system. It will manage all flash block including user data space and spare block.

The Micro SD also contains a sophisticated defect and error management system. It does a read after write under margin conditions to verify that the data is written correctly (except in the case of write pre-erased sectors). In case that a bit is found to be defective, the SD will replace this bad bit with a spare bit within the sector header. If necessary, the Micro SD will even replace the entire sector with a spare sector. This is completely transparent to the master (host device) and does not consume any user data space.

1.2.2 Powerful ECC Algorithms

The powerful ECC algorithms will enhance flash block use rate and whole device life. The SD controller has an innovative algorithm to detect, correct and/or recover the data.

1.2.3 Power Management

A power saving feature of the Micro SD is automatic entrance and exit from sleep mode. Upon completion of an operation, the SD will enter the sleep mode to conserve power if no further commands are received within X seconds, where X is programmable by software. The master does not have to take any action for this to occur. The SD is in sleep mode except when the host is accessing it, thus conserving power.

Any command issued by the master to the Micro SD will cause it to exit sleep mode and response to the master.

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2. Electrical characteristics

2.1 Card Architecture
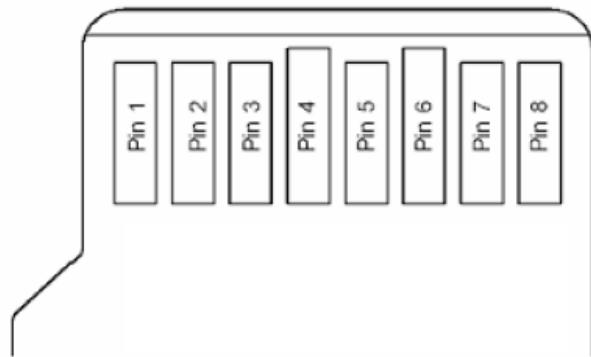
2.2 Pin Assignment

Pin	SD Mode		SPI Mode	
	Name	**Description**	**Name**	**Description**
1	DAT2	Data line[bit 2]	Reserved	
2	CD/DAT3 [2]	Card Detect/Data line [bit 3]	CS	Chip select
3	CMD	Command/Response	DI	Data in
4	VDD	Supply voltage	VDD	Supply voltage
5	CLK	Clock	SCLK	Clock
6	VSS	Supply voltage ground	VSS	Supply voltage ground
7	DAT0	Data line[bit 0]	DO	Data out
8	DAT1	Data line[bit 1]	Reserved	

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2.3 Capacity Specification

The following table shows the specific capacity for the SD 3.0 card (designed with 24nm MLC flash).

Capacity	Total (LBA) Sectors	Total Partition Sectors	User Data Sectors	User Data Bytes
4 GB	7,774,208	7,766,016	7,757,824	3,972,005,888
8 GB	15,564,800	15,556,608	15,548,416	7,960,788,992
16 GB	31,260,672	31,252,480	31,244,288	15,997,075,456

2.4 Performance

Performances of the SD 3.0 card are shown in the table below.

Modes \ Capacity	4 GB	8 GB	16 GB
Read (MB/s)	18	20	19
Write (MB/s)	11	14	13

Note: results may vary depending on settings and platforms.

2.5 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Power Supply Voltage	2.7	3.6	V
V_{DD}-V_{SS}	DC Power Supply Voltage	-0.3	+3.3	V
V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V

2.6 Power consumption (typical)

Modes	Max Read (mA)	Max Write (mA)	Power On	Stand By
Single flash (1x8bit)*	100@ 3.6V	100@ 3.6V	150(uA)	150(uA)

*Data transfer mode in single channel

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3. Physical Characteristics

3.1 Physical Dimension

Reserved for Future Use

VIEW A

CONTACT SURFACE

DETAIL A

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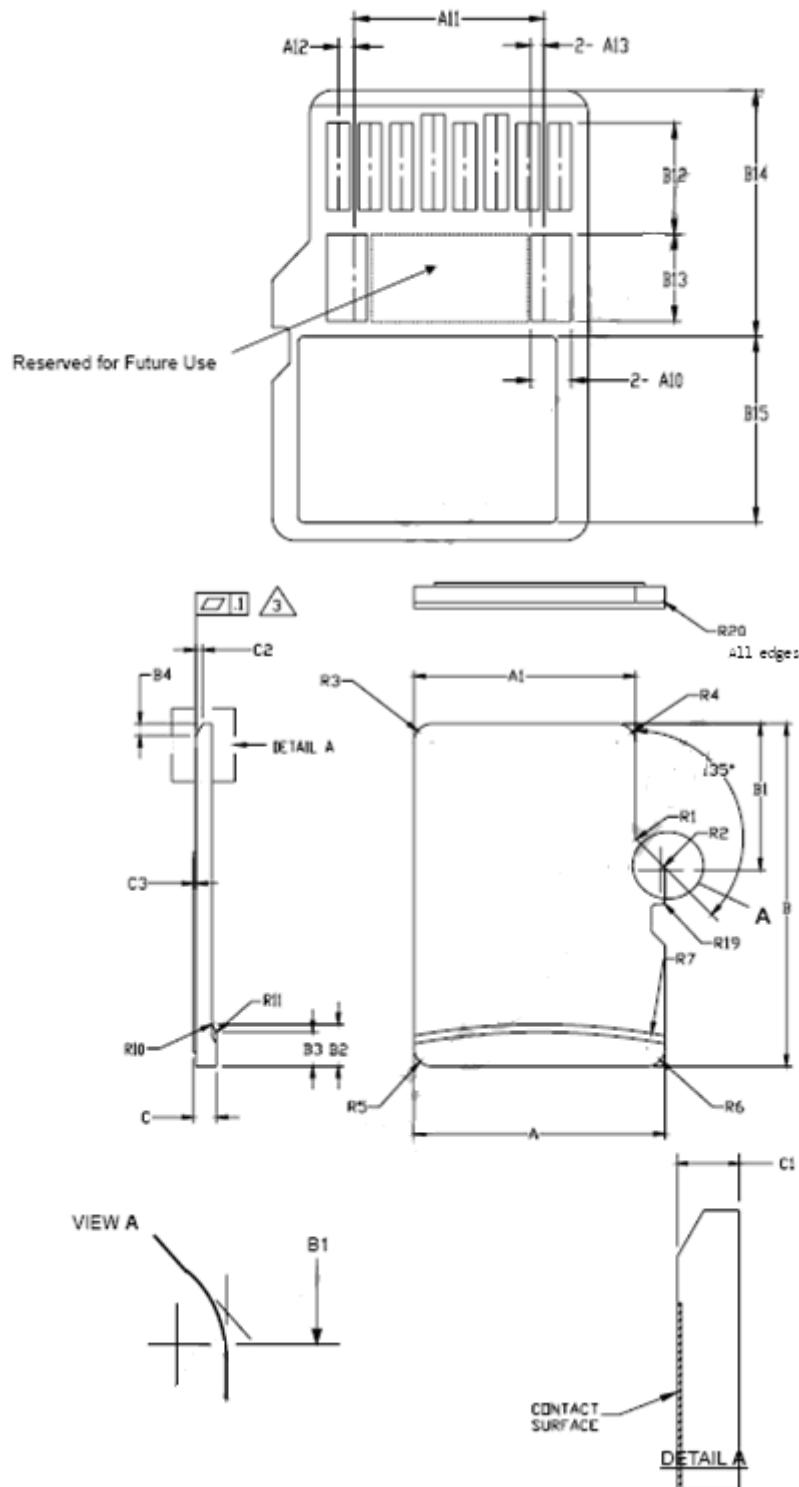
	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

2. DIMENSIONS ARE IN MILLIMETERS.

⚠3. COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

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3.2 Environmental Specifications

Climatic Testing			
Test Item	**DUT State**	**Test Condition (Gold Series)**	
		Temperature	**Duration**
High Temperature	Storage	85℃	500 Hours
	Operation	85℃	168 Hours
Low Temperature	Storage	- 40℃	300 Hours
	Operation	- 25℃	168 Hours
High Temperature & High Humidity	Storage	40℃ 95%	500 Hours
	Operation	40℃ 95%	4 Hour
Thermal Cycling	Storage*	- 40℃ ~ 85℃ 30min hold each	20 Cycles

Durability Testing	
Test Item	**Descriptions**
Insertion/Removal	10,000 cycles

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Bending	10nt/Stimes for 6 faces and 4 corners (each drop was performed 3 times, total of 30 drops)
Electrostatic Discharge	Contact discharge: HCP & VCP Air discharge:　　ALL – VSS (±), 　　　　　　　　　ALL – VCC (±) 　　　　　　　　　VCC – VSS (±), 　　　　　　　　　ALL – ALL (±)
Ultraviolet Radiation	Units are non-operating. UVB bandwidth：313nm. Test irradiation：0.63 w/m²/nm. Radiation cycle：Radiation on for 4 hours at temperature 60°C, then radiation off for 4 hours at temperature 50°C. Number of cycle：6 cycles. Duration of test：48 hours
Drop	1.Sm free fall, 10times
Salt Water Spray	3+/-1%NaCl; 35℃; 24hrs
Torque	0.SN-m or 0.2Sdegree S time; 30sec/direction

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4. AC Characteristics

4.1 Micro SD Interface Timing (Default)
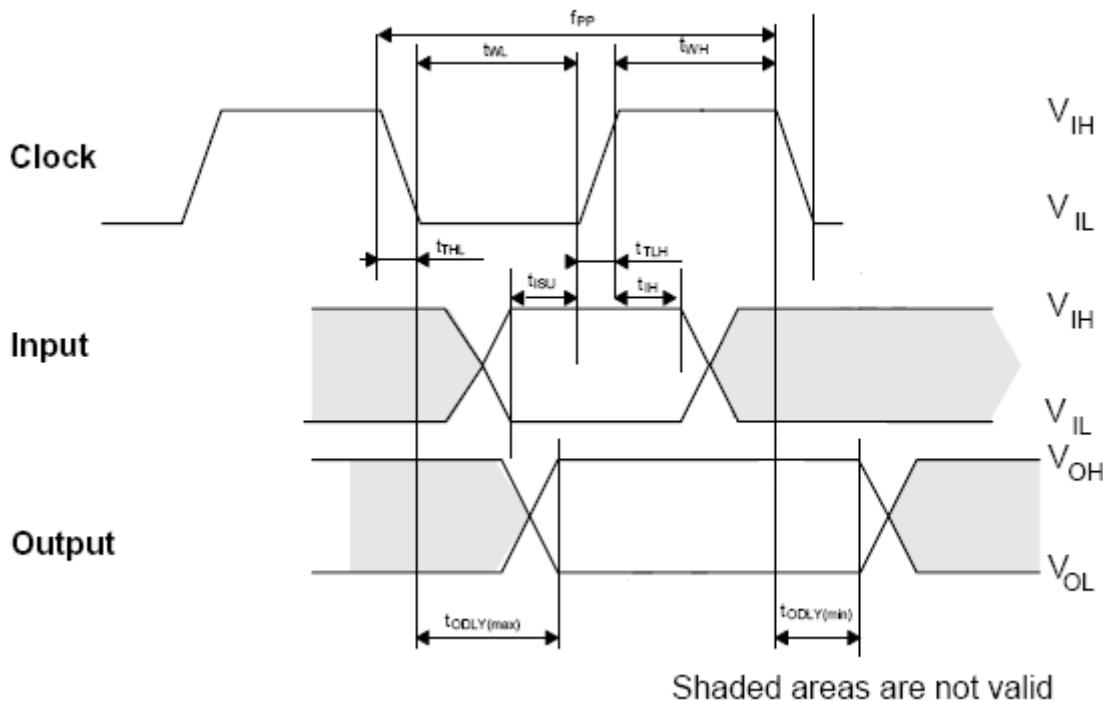
Shaded areas are not valid

SYMBOL	PARAMETER	MIN	MAX	UNIT	Note
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
f_{PP}	Clock frequency Data Transfer Mode	0	25	MHz	$C_{card} \leq 10$ pF (1 card)
f_{OD}	Clock frequency Identification Mode	$0_{(1)}$/100	400	kHz	$C_{card} \leq 10$ pF (1 card)
t_{WL}	Clock low time	10	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{WH}	Clock high time	10	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{TLH}	Clock rise time	-	10	ns	$C_{card} \leq 10$ pF (1 card)
t_{THL}	Clock fall time	-	10	ns	$C_{card} \leq 10$ pF (1 card)
t_{ISU}	Input setup time	5	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{IH}	Input hold time	5	-	ns	$C_{card} \leq 10$ pF (1 card)

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t_{ODLY}	Output delay time	0	14	ns	$C_L \leq 40$ pF (1 card)
tODLY	Output Delay time during Identification Mode	0	50	ns	$C_L \leq 40$ pF (1 card)

(1)0Hz means to stop the clock. The given minimum frequency range is for cases that requires the clock to be continued.

## 4.2 Micro SD Interface Timing (High Speed Mode)
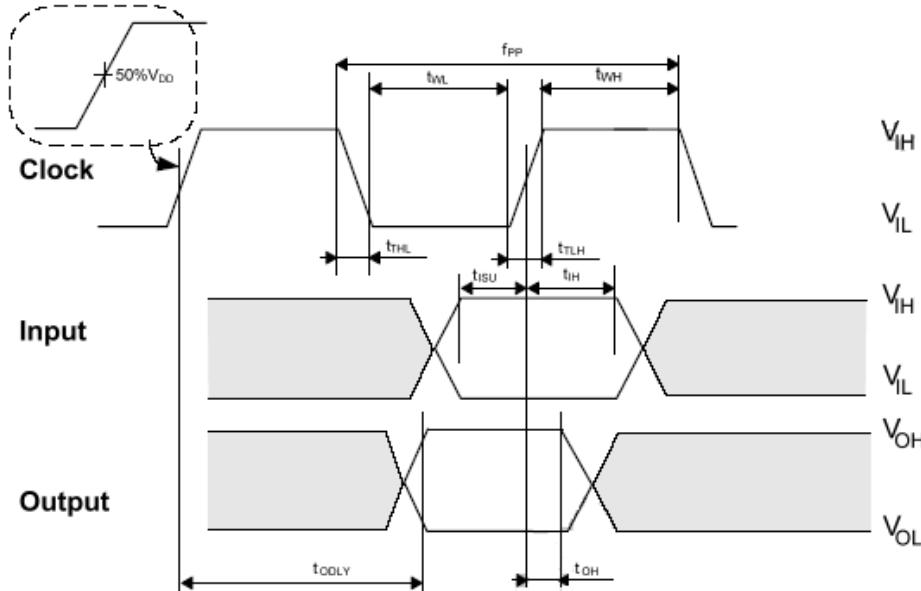
Shaded areas are not valid

| SYMBOL	PARAMETER	MIN	MAX	UNIT	Note
f_{PP}	Clock frequency data transfer mode	0	50	MHz	Ccard≤10 pF (1 card)
t_{WL}	Clock low time	7	-	ns	Ccard≤10 pF (1 card)
t_{WH}	Clock high time	7	-	ns	Ccard≤10 pF (1 card)
t_{TLH}	Clock rise time	-	3	ns	Ccard≤10 pF (1 card)
t_{THL}	Clock fall time	-	3	ns	Ccard≤10 pF (1 card)
t_{ISU}	Input setup time	6	-	ns	Ccard≤10 pF (1 card)
t_{IH}	Input hold time	2	-	ns	Ccard≤10 pF (1 card)
t_{ODLY}	Output delay time		14	ns	CL≤40 pF (1 card)
T_{OH}	Output hold time	2.5	50	ns	CL≤15 pF (1 card)
C_L	System capacitance of each line*		40	pF	CL≤15 pF (1 card)

*In order to satisfy severe timing, host shall run on only one card

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4.3 SD Interface Timing (SDR12, SDR25 and SDR50 Modes) Input

Symbol	Min	Max	Unit	Remark
tCLK	4.80	-	ns	208MHz (Max.), Between rising edge, VCT= 0.975V
tCR, tCF	-	0.2* tCLK	ns	tCR, tCF < 2.00ns (max.) at 100MHz, CCARD=10pF
Clock Duty	30	70	%	
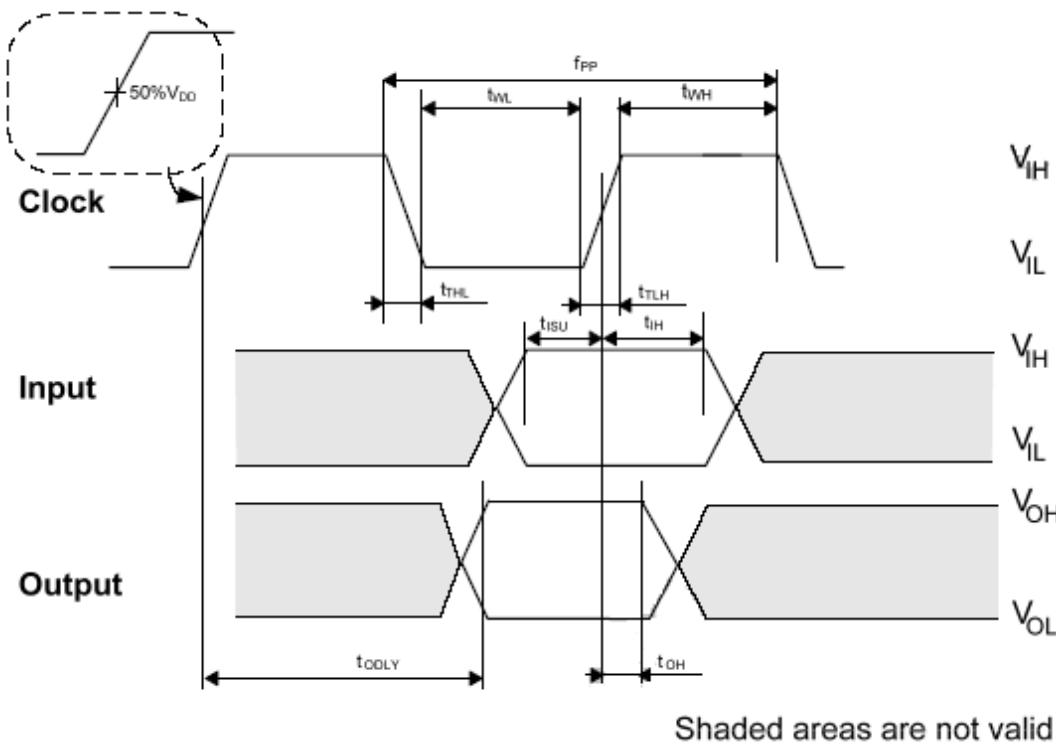
Shaded areas are not valid

4.3.1 SDR50 Input Timing

Card Input Timing

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Symbol	Min	Max	Unit	SDR50 Mode
tIs	3.00	-	ns	CCARD =10pF, VCT= 0.975V
tIH	0.80	-	ns	CCARD =5pF, VCT= 0.975V

4.3.2 Output
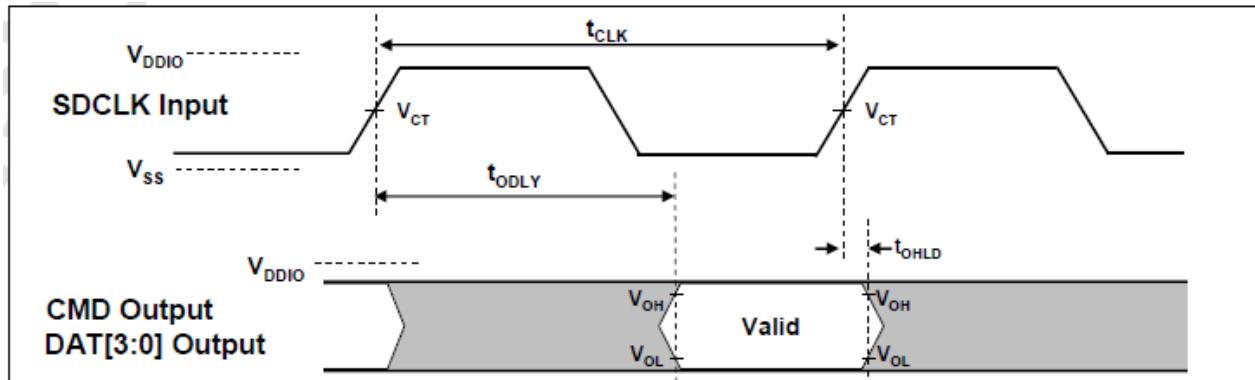
Output Timing of Fixed Data Window

Symbol	Min	Max	Unit	Remark
tODLY	-	7.5	ns	tCLK>=10.0ns, CL=30pF, using driver Type B, for SDR50
tODLY	-	14	ns	tCLK>=20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12,
TOH	1.5	-	ns	Hold time at the tODLY (min.), CL=15pF

4.3.3 SD Interface Timing (DDR50 Mode)
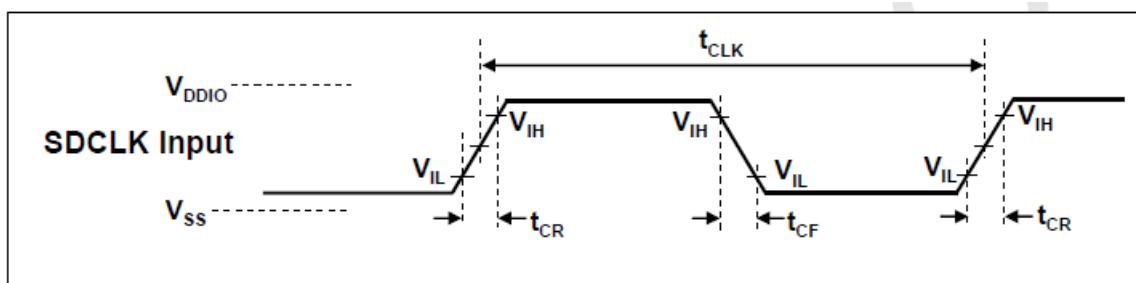
Clock Signal Timing

| Symbol	Min	Max	Unit	Remark
tCLK	20	-	ns	50MHz (Max.), Between rising edge
tCR, tCF	-	0.2* tCLK	ns	tCR, tCF < 4.00ns (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	

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Access the best
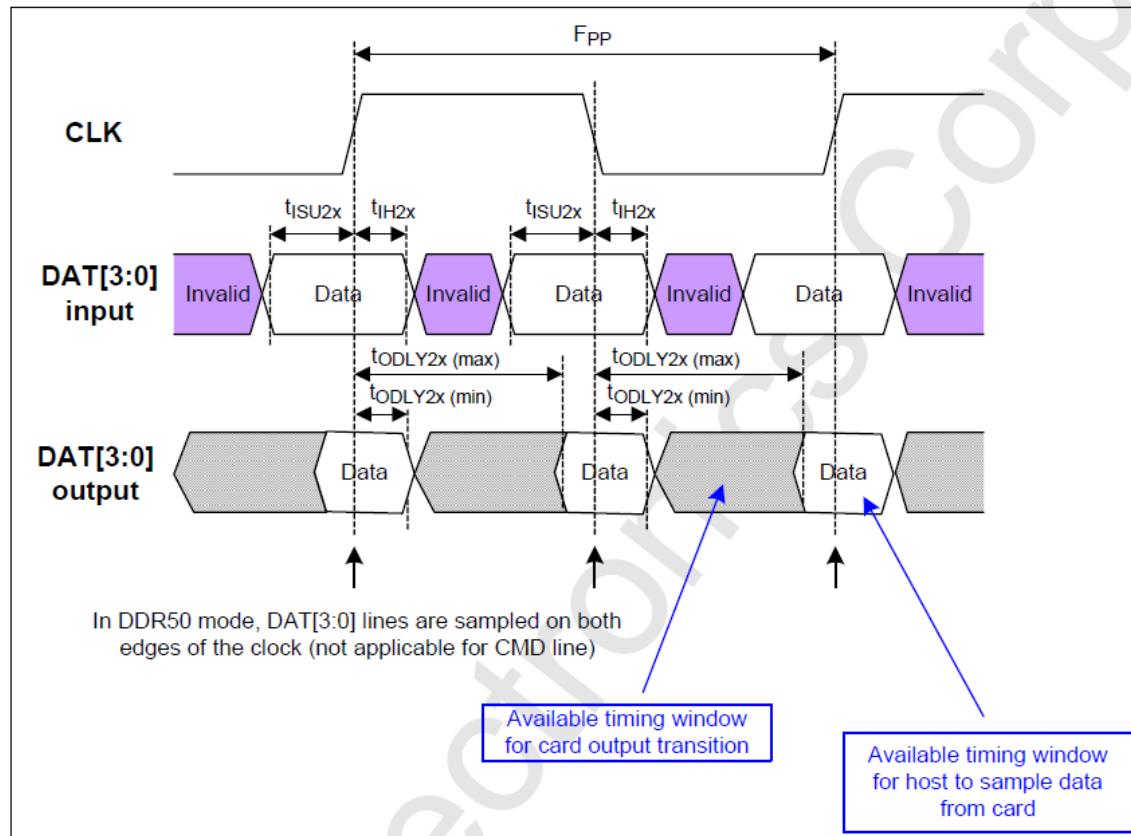
Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

4.3.4 Bus Timings – Parameters Values (DDR50 Mode)

Symbol	Parameters	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
t_{ISU}	Input set-up time	6	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{IH}	Input hold time	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Output CMD (referenced to CLK rising edge)					
t_{ODLY}	Output Delay time during Data Transfer Mode	-	13.7	ns	$C_L \leq 30$ pF (1 card)
T_{OH}	Output Hold time	1.5	-	ns	$C_L \geq 15$ pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
t_{ISU2x}	Input set-up time	3	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{IH2x}	Input hold time	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
t_{ODLY2x}	Output Delay time during Data Transfer Mode	-	7.0	ns	$C_L \leq 25$ pF (1 card)
T_{OH2x}	Output Hold time	1.5	-	ns	$C_L \geq 15$ pF (1 card)

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5. Product Ordering Information

5.1 Product Code Designations

A P – MSD x x x C X 4 P – X XX

Flash Type:
TM: Toshiba MLC

F/W

CTL Solution

4: SDHC

Configuration
S: Single Chip
D: Two chips
H: four chips

Temperature:
C: Commercial Temperature

Capacities:
04G: 4GB
08G: 8GB
16G: 16GB

Model Name

Apacer Product Code

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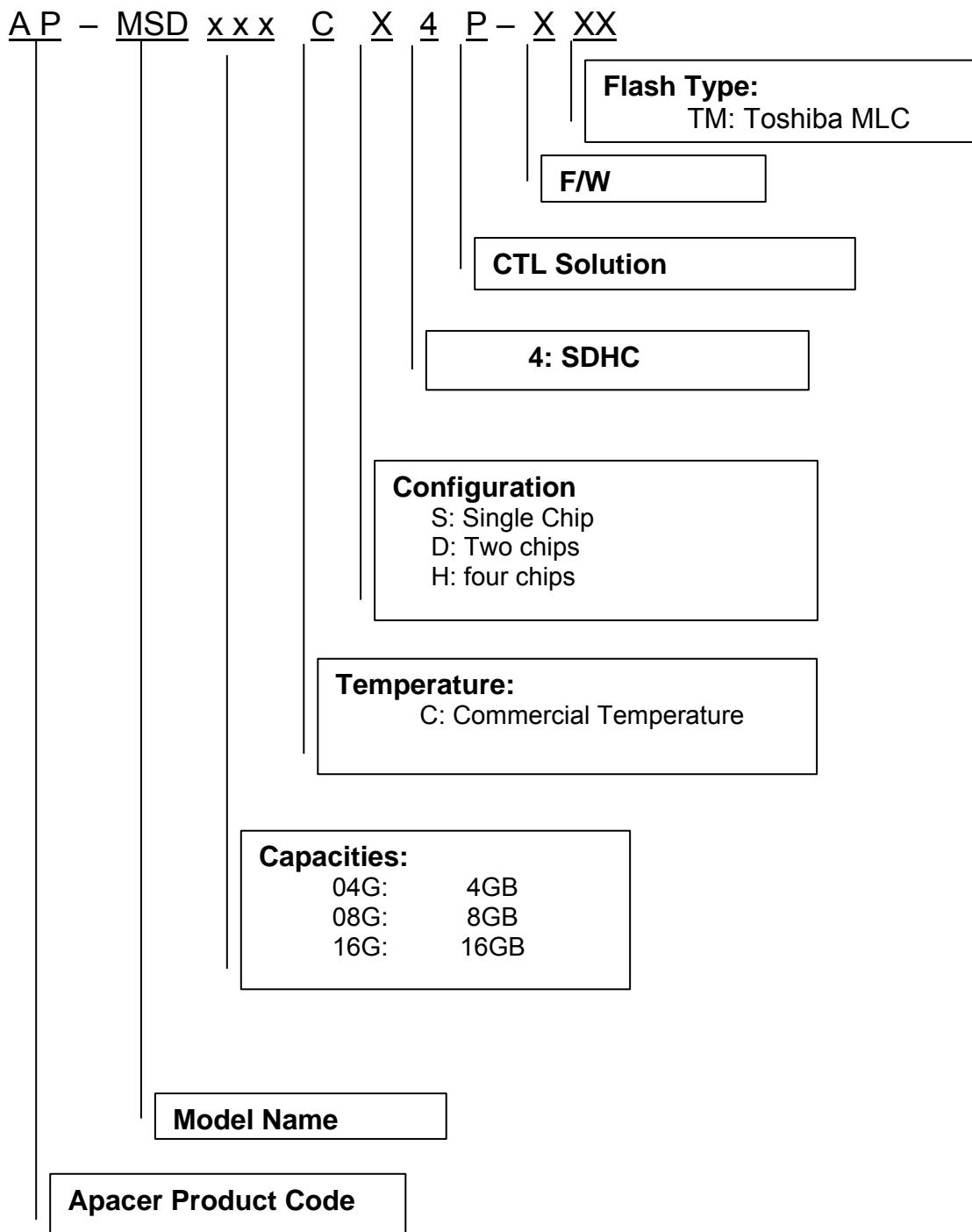
5.2 Valid Combinations

Capacity	AP/N
4 GB	AP- MSD04GCS4P-TM
8 GB	AP-MSD08GCD4P-TM
16 GB	AP-MSD16GCH4P-TM

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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Revision History

Revision	Description	Date
0.1	Preliminary	08/24/2011
0.2	Added Durability Testing -- items and descriptions of Durability Testing have been added	08/29/2011
0.3	Added 8/16 GB to the capacity	09/06/2011
1.0	Official release	11/03/2011

Global Presence

Taiwan (Headquarters)

Apacer Technology Inc.
4th Fl., 75 Hsin Tai Wu Rd., Sec.1
Hsichih, New Taipei City
Taiwan 221
R.O.C.
Tel: +886-2-2698-2888
Fax: +886-2-2698-2889
amtsales@apacer.com

U.S.A.

Apacer Memory America, Inc.
386 Fairview Way, Suite102,
Milpitas, CA 95035
Tel: 1-408-518-8699
Fax: 1-408-935-9611
sa@apacerus.com

Japan

Apacer Technology Corp.
5F, Matsura Bldg., Shiba, Minato-Ku
Tokyo, 105-0014, Japan
Tel: 81-3-5419-2668
Fax: 81-3-5419-0018
jpservices@apacer.com

Europe

Apacer Technology B.V.
Aziëlaan 22,
5232 BA 's-Hertogenbosch,
The Netherlands
Tel: 31-73-645-9620
Fax: 31-73-645-9629
sales@apacer.nl

China

Apacer Electronic (Shanghai) Co., Ltd
1301, No.251,Xiaomuqiao Road, Shanghai,
200032, China
Tel: 86-21-5529-0222
Fax: 86-21-5206-6939
sales@apacer.com.cn

India

Apacer Technologies Pvt Ltd,
#1064, 1st Floor, 7th 'A' Main,
3rd Block Koramangala, Bangalore – 560 034
Tel: +91 80 4152 9061/62/63
Fax: +91 80 4170 0215
sales_india@apacer.com

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